FAIRCHILD SEMICONDUCTOR®

September 2003

FDP3672

N-Channel PowerTrench® MOSFET
105V, 41A, 33mΩ

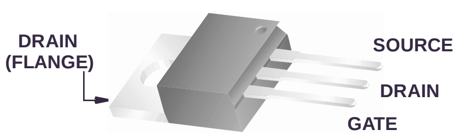
Features

- $r_{DS(ON)}$ = 25mΩ (Typ.), V_{GS} = 10V, I_D = 41A
- Q_g(tot) = 28nC (Typ.), V_{GS} = 10V
- Low Miller Charge
- Low Q_{RR} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101

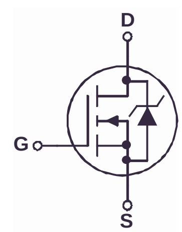
Formerly developmental type 82760

Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42V Automotive Load Control
- Electronic Valve Train Systems



TO-220AB
FDP SERIES



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	105	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, V_{GS} = 10V)	41	A
	Continuous (T_C = 100°C, V_{GS} = 10V)	31	A
	Continuous (T_{amb} = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 62°C/W)	5.9	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	48	mJ
P_D	Power dissipation	135	W
	Derate above 25°C	0.9	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	^{o}C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220	1.11	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220 (Note 2)	62	^{o}C/W

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP3672	FDP3672	TO-220AB	Tube	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	105	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 80V, V_{GS} = 0V, T_C= 150°C	-	-	250	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 41A, V_{GS} = 10V	-	0.025	0.033	Ω
		I_D = 21A, V_{GS} = 6V,	-	0.031	0.055	Ω
		I_D = 41A, V_{GS} = 10V, T_C = 175°C	-	0.063	0.070	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	1670	-	pF
C_{OSS}	Output Capacitance		-	240	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	55	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 50V, I_D = 41A, I_g = 1.0mA	-	28	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V	-	3.9	5	nC
Q_{gs}	Gate to Source Gate Charge		-	12	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	8.0	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	6.5	-	nC
Resistive Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 50V, I_D = 41A, V_{GS} = 10V, R_{GS} = 11.0Ω	-	-	90	ns
$t_{d(ON)}$	Turn-On Delay Time		-	12	-	ns
t_r	Rise Time		-	48	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	24	-	ns
t_f	Fall Time		-	27	-	ns
t_{OFF}	Turn-Off Time		-	-	77	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 41A	-	-	1.25	V
		I_{SD} = 21A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 41A, dI_{SD}/dt =100A/µs	-	-	39	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 41A, dI_{SD}/dt =100A/µs	-	-	42	nC

Notes:
1: Starting T_J = 25°C, L = 0.11mH, I_{AS} = 30A.
2: Pulse Width = 100s

Typical Characteristics T_C = 25°C unless otherwise noted

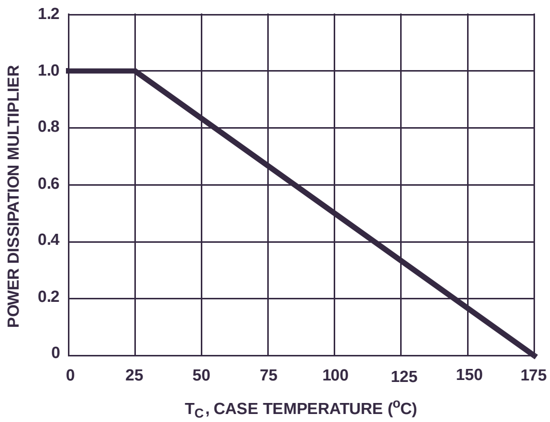


Figure 1. Normalized Power Dissipation vs Ambient Temperature

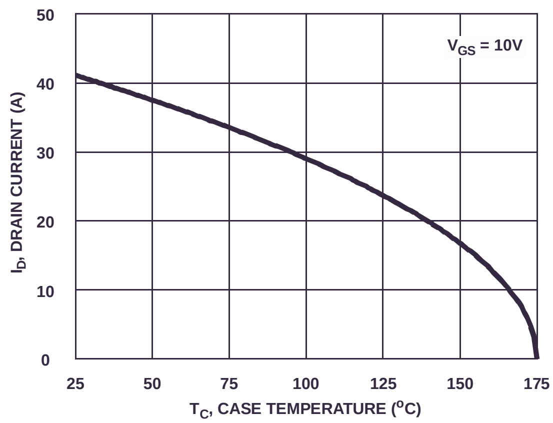


Figure 2. Maximum Continuous Drain Current vs Case Temperature

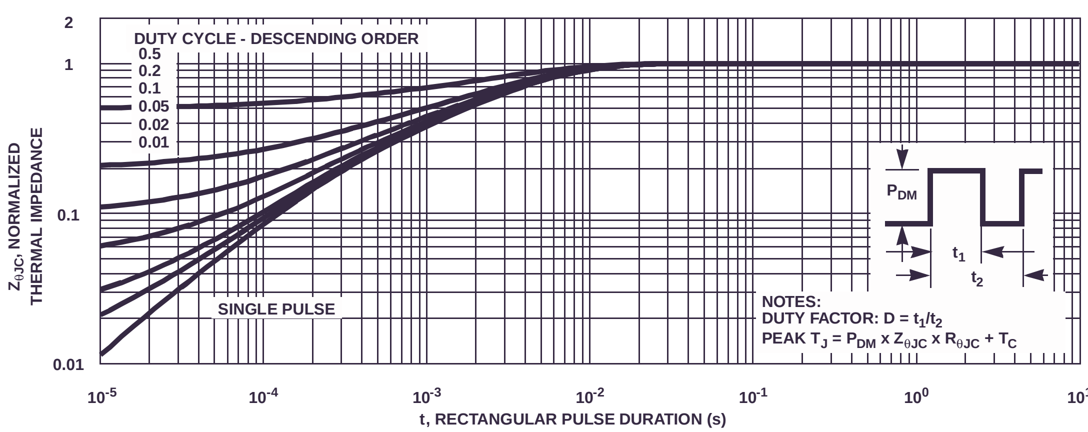


Figure 3. Normalized Maximum Transient Thermal Impedance

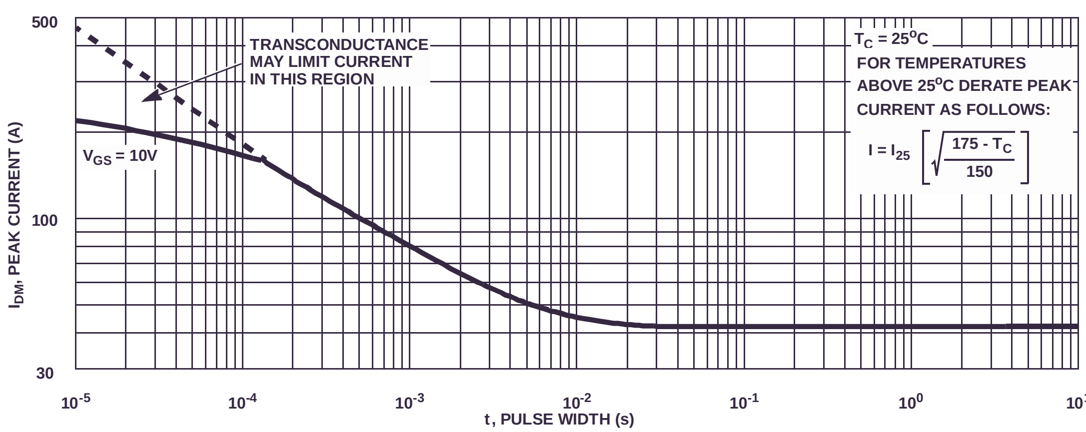


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

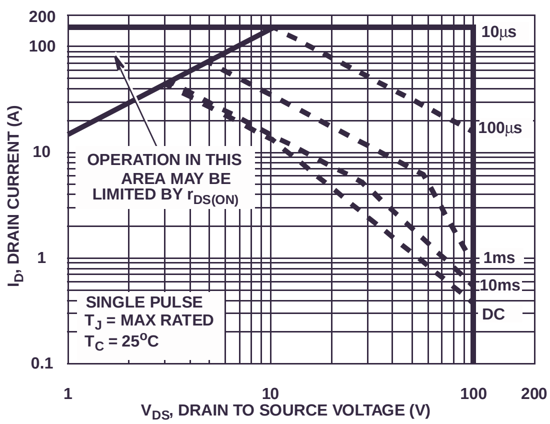
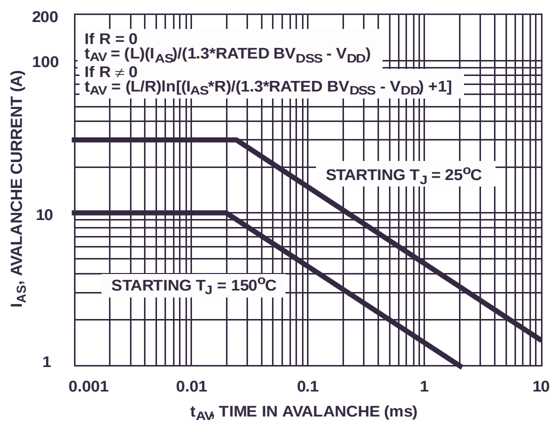


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

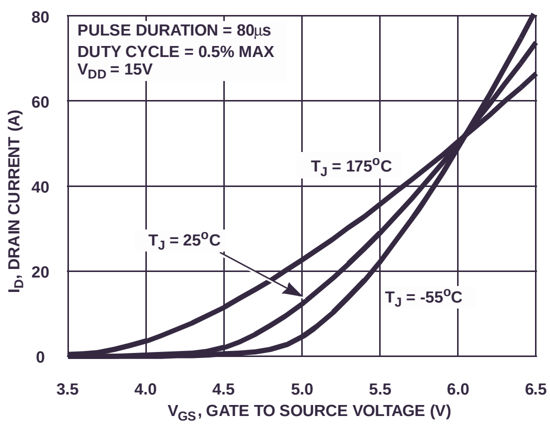


Figure 7. Transfer Characteristics

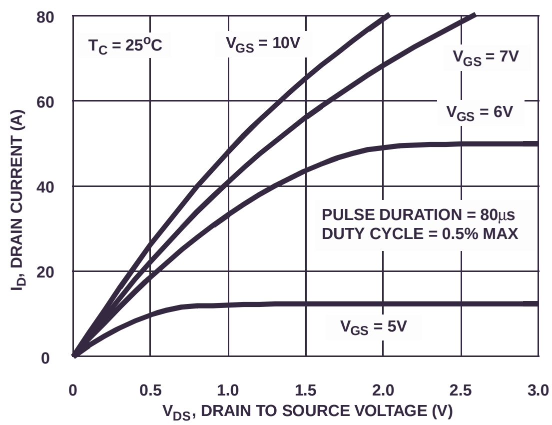


Figure 8. Saturation Characteristics

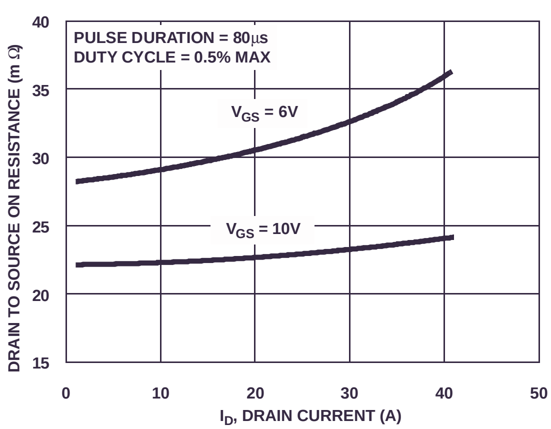


Figure 9. Drain to Source On Resistance vs Drain Current

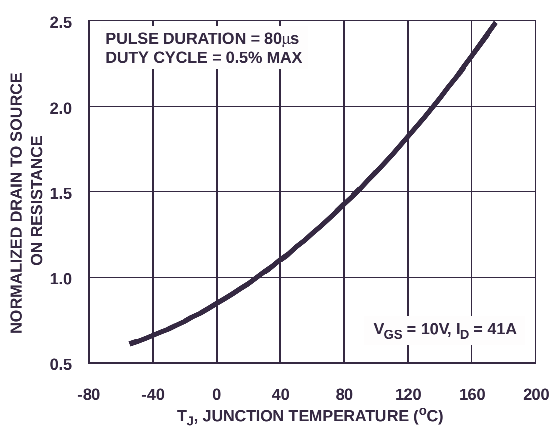


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted

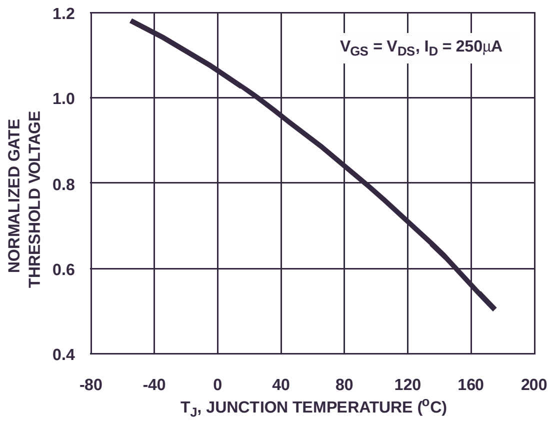


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

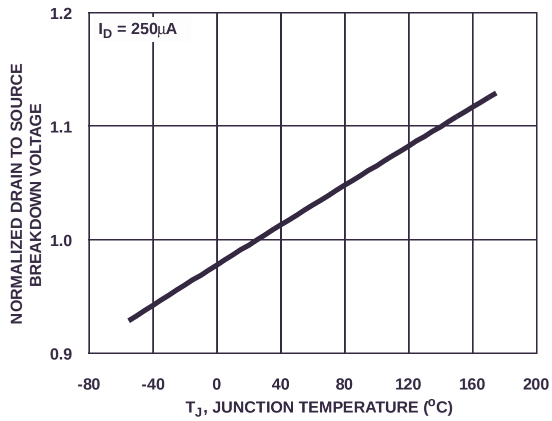


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

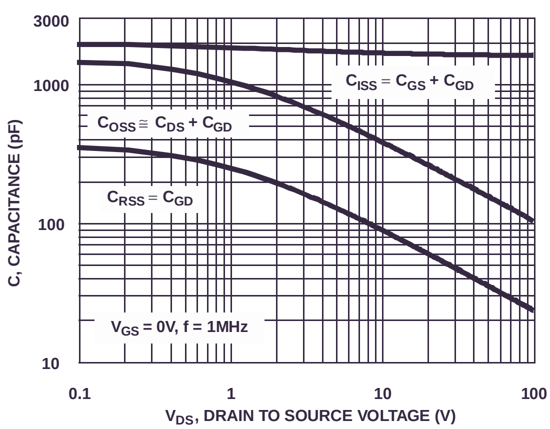


Figure 13. Capacitance vs Drain to Source Voltage

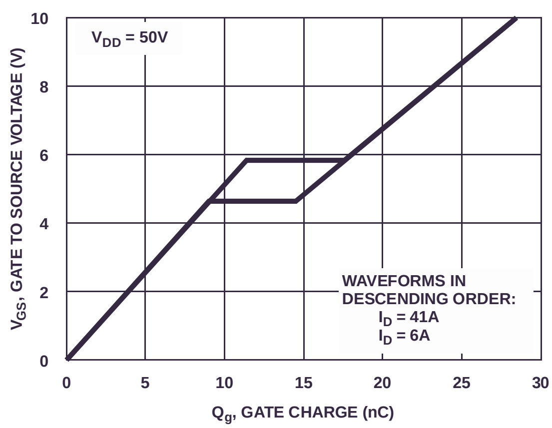


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

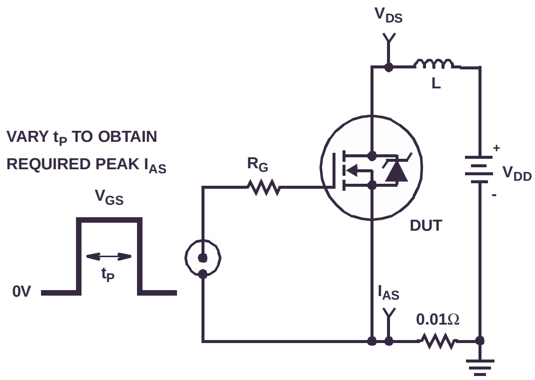


Figure 15. Unclamped Energy Test Circuit

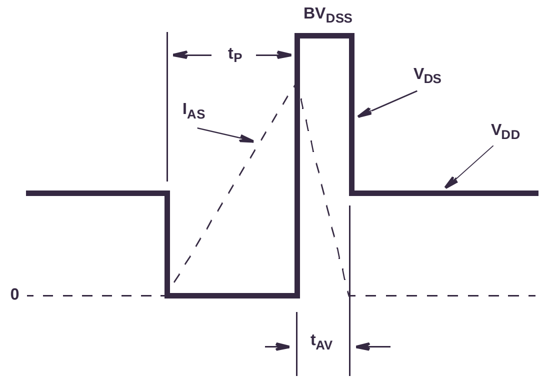


Figure 16. Unclamped Energy Waveforms

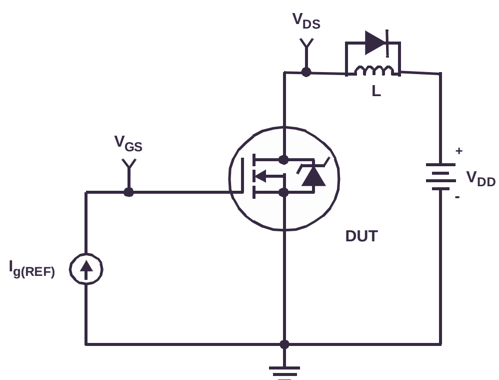


Figure 17. Gate Charge Test Circuit

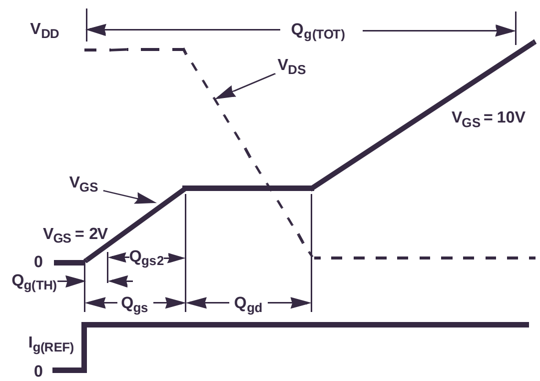


Figure 18. Gate Charge Waveforms

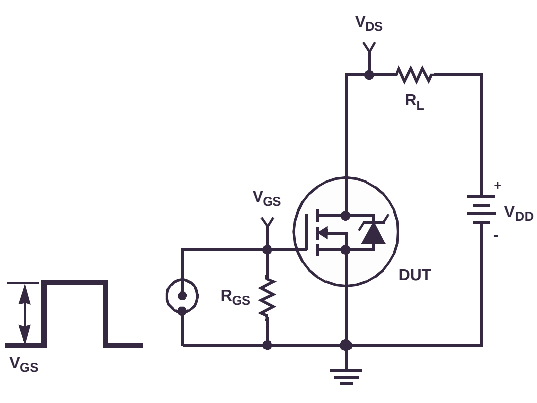


Figure 19. Switching Time Test Circuit

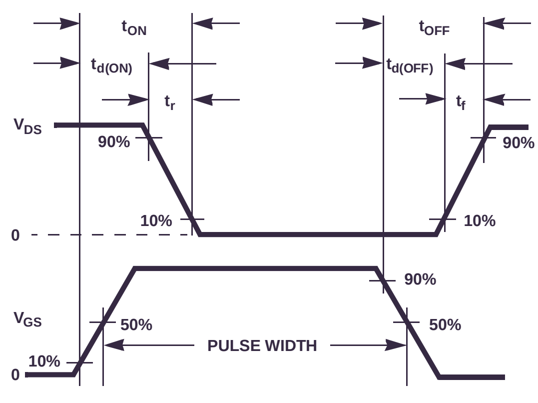


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

```
.SUBCKT FDP3672 2 1 3 ;       rev October 2002
Ca  12  8 5.8e-10
Cb 15 14 6.8e-10
Cin 6 8 1.6e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 105
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 9.56e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 4.45e-9

RLgate 1 9 95.6
RLdrain 2 5 10
RLsource 3 7 44.5

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 6.0e-3
Rgate 9 20 1.5
RSLC1 5 51 RSLCMOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 9.5e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1
ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*98),3))}

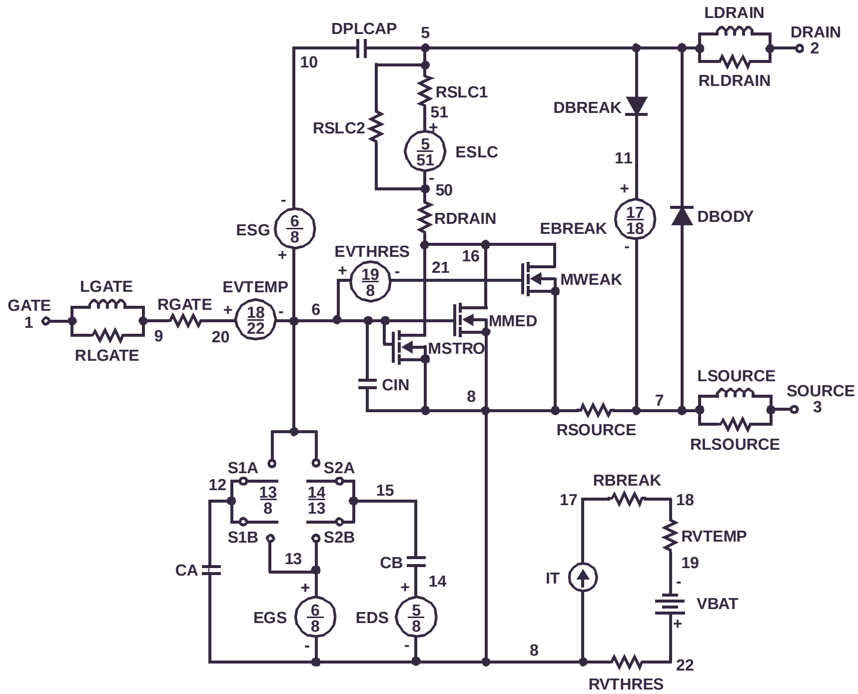
.MODEL DbodyMOD D (IS=1.0E-11 N=1.05 RS=3.7e-3 TRS1=2.5e-3 TRS2=1.0e-6
+ CJO=1.2e-9 M=0.58 TT=3.75e-8 XTI=4.0)
.MODEL DbreakMOD D (RS=15 TRS1=4.0e-3 TRS2=-5.0e-6)
.MODEL DplcapMOD D (CJO=3.8e-10 IS=1.0e-30 N=10 M=0.60)

.MODEL MmedMOD NMOS (VTO=3.6 KP=3 IS=1e-40 N=10 TOX=1 L=1u W=1u RG=1.5)
.MODEL MstroMOD NMOS (VTO=4.3 KP=59 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=3.09 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=15 RS=0.1)

.MODEL RbreakMOD RES (TC1=9.0e-4 TC2=-1.0e-7)
.MODEL RdrainMOD RES (TC1=11.0e-3 TC2= 6.1e-5)
.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=1.0e-6)
.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)
.MODEL RvthresMOD RES (TC1=-3.5e-3 TC2=-1.5e-5)
.MODEL RvtempMOD RES (TC1=-4.3e-3 TC2=1.5e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-3.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-5.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)

.ENDS
```



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV October 2002
template FDP3672 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl=1.0e-11,nl=1.05,rs=3.7e-3,trs1=2.5e-3,trs2=1.0e-6,cjo=1.2e-9,m=0.58,tt=3.75e-8,xti=4.0)
dp..model dbreakmod = (rs=15,trs1=4.0e-3,trs2=-5.0e-6)
dp..model dplcapmod =  (cjo=3.8e-10,isl=10.0e-30,nl=10,m=0.60)
m..model mmedmod = (type=_n,vto=3.6,kp=3,is=1e-40, tox=1)
m..model mstrongmod = (type=_n,vto=4.3,kp=59,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.09,kp=0.05,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-5.0,voff=-3.5)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-3.5,voff=-5.0)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-0.5,voff=0.3)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=0.3,voff=-0.5)
c.ca n12 n8 = 5.8e-10
c.cb n15 n14 = 6.8e-10
c.cin n6 n8 = 1.6e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 105
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

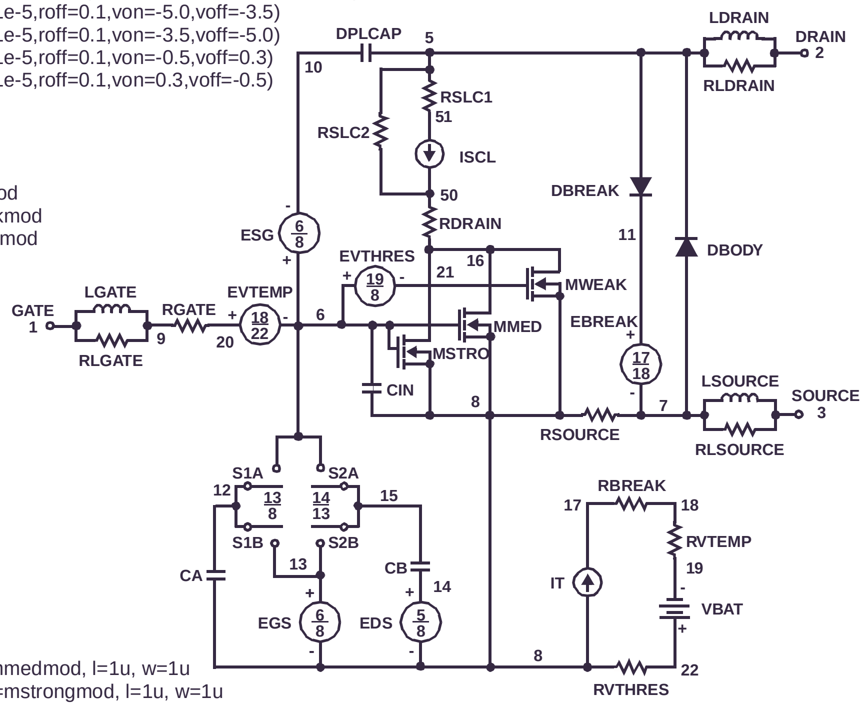
l.lgate n1 n9 = 95.6e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 4.45e-9

res.rlgate n1 n9 = 9.56
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 44.5

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=9.0e-4,tc2=-1.0e-7
res.rdrain n50 n16  = 6.0e-3, tc1=11.0e-3,tc2=6.1e-5
res.rgate n9 n20 = 1.5
res.rslc1 n5 n51  = 1.0e-6, tc1=3.0e-3,tc2=1.0e-6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7  = 9.5e-3, tc1=4.0e-3,tc2=1.0e-6
res.rvthres n22 n8  = 1, tc1=-3.5e-3,tc2=-1.5e-5
res.rvtemp n18 n19  = 1, tc1=-4.3e-3,tc2=1.5e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/98))** 3))
}
```



SPICE Thermal Model

REV October 2002

FDP3672

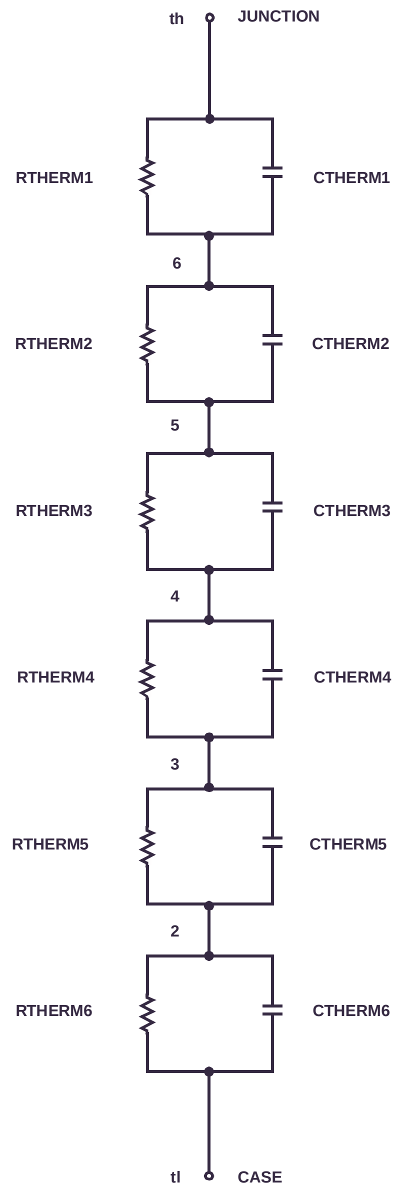
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CTHERM1 TH 6 3.2e-3
CTHERM2 6 5 3.3e-3
CTHERM3 5 4 3.4e-3
CTHERM4 4 3 3.5e-3
CTHERM5 3 2 6.4e-3
CTHERM6 2 TL 1.9e-2

RTHERM1 TH 6 5.5e-4
RTHERM2 6 5 5.0e-3
RTHERM3 5 4 4.5e-2
RTHERM4 4 3 10.5e-2
RTHERM5 3 2 3.4e-1
RTHERM6 2 TL 3.5e-1
```

SABER Thermal Model

```
SABER thermal model FDP3672
template thermal_model th tl
thermal_c th, tl
{
cctherm.ctherm1 th 6 =3.2e-3
ctherm.ctherm2 6 5 =3.3e-3
ctherm.ctherm3 5 4 =3.4e-3
ctherm.ctherm4 4 3 =3.5e-3
ctherm.ctherm5 3 2 =6.4e-3
ctherm.ctherm6 2 tl =1.9e-2

rtherm.rtherm1 th 6 =5.5e-4
rtherm.rtherm2 6 5 =5.0e-3
rtherm.rtherm3 5 4 =4.5e-2
rtherm.rtherm4 4 3 =10.5e-2
rtherm.rtherm5 3 2 =3.4e-1
rtherm.rtherm6 2 tl =3.5e-1
}
```



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FACT Quiet Series™
FAST®
FASTr™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
I^2C™
ImpliedDisconnect™
ISOPLANAR™
Across the board. Around the world.™
The Power Franchise™
Programmable Active Droop™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic®
TINYOPTO™
TruTranslation™
UHC™
UltraFET®
VCX™

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.